UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/763,251	01/26/2004	Yuan-Mou Su	0941-0900P	8018

2292 7590 12/01/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,251	SU, YUAN-MOU	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on January 26, 2004.

2. Claims 1 – 7 are pending in this case. Claims 1 and 4 are independent claims.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwata et al. U.S. Patent No. 5,652,729 – filed Feb. 6, 1996.

Regarding independent claim 1, Fig. 16 of Iwata et al. discloses a method for generating a refresh clock of a DRAM module (Col. 1 lines 6 – 10), wherein the DRAM module comprises a plurality of memory cells ((Fig. 1 [Memory Cell]), each of the memory cells having a storage capacitor (Col. 3 lines 53 – 57 and Col. 10 lines 50 – 54), comprising: providing a dummy capacitor (Fig. 16 [203]; Col. 1 lines 64 – 66 disclosing capacitor 203 is a storage element of a dummy memory cell, therefore 203 is

a dummy capacitor), the dummy capacitor has a positive correlation with the storage capacitor (Col. 10 lines 54 – 56 disclosing the dummy memory cell of refresh timer having the same structure as of the main memory cell; therefore the capacitor of the dummy cell and the capacitor of the main memory cell are positive correlation); and generating a refresh clock according to a capacitance of the dummy capacitor (Col. 2 lines 9 – 14); wherein a refresh interval of the refresh clock is positively correlated with the capacitance of the dummy capacitor (this is inherent characteristic for refresh interval and capacitance of capacitor 203 taught by Iwata et al. because the interval of the refresh clock are determining by the capacitance of the dummy capacitor 203; if the capacitance of the capacitor 203 increase, then the interval for refreshing clock must be increase in order to refresh the capacitor up to its capacitance).

Regarding dependent claim 2, Fig. 16 of Iwata et al. further providing an oscillator [209] for generating the refresh clock, wherein the dummy capacitor is an oscillator load [203].

Regarding dependent claim 3, Iwata discloses wherein the dummy capacitor [203] is one of the storage capacitors (Col. 1 lines 64 – 67).

Regarding independent claim 4, Fig. 16 of Iwata et al. discloses refresh clock generator of a DRAM module (Col. 1 lines 6 – 10), wherein the DRAM module comprises a plurality of memory cells (Fig. 1 [Memory Cell]), each of the memory cells having a storage capacitor (Col. 10 lines 50 – 51), comprising: a dummy capacitor (Fig. 16 [203] Col. 1 lines 64 – 66 disclosing capacitor [203] is a storage element of a dummy memory cell, therefore 203 is a dummy capacitor) positively correlated with the storage

capacitor (Col. 10 lines 54 – 56 disclosing the dummy memory cell of refresh timer having the same structure as of the main memory cell; therefore the capacitor of the dummy cell and the capacitor of the main memory cell are positive correlation); and a clock generator (Fig. 16 [209]) for generating a refresh clock (Fig. 16 [OUT]), and coupling to the dummy capacitor (Fig. 16 [203]); wherein a refresh interval of the refresh clock is positively correlated with a capacitance of the dummy capacitor (this is inherent characteristic for interval of refresh clock [OUT] and capacitance of capacitor [203] taught by Iwata et al. because the interval of the refresh clock are determining by the capacitance of the dummy capacitor 203; if the capacitance of the capacitor [203] increase, then the interval for refreshing clock must be increase in order to refresh the capacitor up to its capacitance).

Regarding dependent claim 7, Iwata discloses wherein the dummy capacitor is one of the storage capacitors (Col. 1 lines 64 – 67).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 - 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al. U.S. Patent No. 5,652,729 – filed Feb. 6, 1996 in view of Lin U.S. Patent No. 5,596,545 filed Dec. 4, 1995.

Regarding dependent claims 5 and 6, Iwata et al. as applied to claims 4 above, fails to disclose wherein the clock generator is a ring oscillator and the dummy capacitor is a ring oscillator load (Claim 5) and wherein the refresh clock generator comprises a plurality of dummy capacitors, the ring oscillator comprises a plurality of inverters, and each output terminal of the inverters couples to a corresponding dummy capacitor (Claim 6).

Fig. 2 of Lin (Col. 6 lines 16 – 27) discloses a the refresh clock generator [20] for DRAM module (Col. 5 line 63); wherein the refresh clock generator [20] is a ring oscillator and the dummy capacitor [34] is a ring oscillator load and wherein the refresh clock generator comprises a plurality of dummy capacitors [34], the ring oscillator comprises a plurality of inverters [24], and each output terminal of the inverters couples to a corresponding dummy capacitor [34].

Iwata et al. and Lin are common subject matter of clock generator for refreshing DRAM module. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the ring oscillator taught by Lin into the oscillator Iwata et al. for the purpose of providing an improved semiconductor memory device with internal self-refreshing and controlling self-refreshing time period (Lin; Col. 4 lines 55 – 60).

Prior art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wahlstrom	Patent No. US 5,375,086	Date of Patent: Dec. 20, 1994
Lee et al.	Pub. No: US 2004/0008558 A1	Pub. Date: Jan. 15, 2004

Contact Information

7. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 11/23/2004

MICHAEL S. LEBENTRITT
PRIMARY EXAMINER